EE/CprE/SE 492 BIWEEKLY REPORT 2

Date: ***September 16th, 2023 – September 27th***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Biweekly Summary

Over the past week and a half, we have made more progress in pushing our devices through the analog process flow. We have identified the issue that was plaguing our post-layout OP-amp design. It most likely had to do with the pins not properly lining up from the original schematic netlist to the post-layout netlist. With this issue identified, we should be able to correct it and get the OP-amp working as intended. We also made progress on our 3-bit ADC and pushed it through the analog process flow. We are currently working on making the layout of this device. We made more progress updating the digital drivers that will work with the harness to push data in and read data out of our design. Finally, we began work on creating the final documentation/guide on how to set everything up for the analog process flow. This is important so that future teams can learn from what we did and have an easier time working on this type of project with the Skywater 130 nm process.

Past Weeks Accomplishments

- Joshua Thater
    - Started work on writing up a guide for setting up an environment for analog design flow, how to configure the tools, and how to push a basic design through the analog process flow

    - Asked in the Slack channel how to write to 1T1R cell and verify that a write occurred.
        - Got a response, and seems like it is possible just haven't had the time to actually test it out myself
- Aiden Petersen
    - Digital Behavioural model bug fixing
        - More accurately modeled the intended ADC quantization done at the input step.
    - Driver implementation
        - Implemented function in C that does read, write, and MAC operations
        - Created a test case using the drivers to multiply a vector by the identity matrix.
- Matt Ottersen
    - Solved issue that simulation of netlist was not matching simulation of Schematic
    - Confirmed layout of Op-Amp works
- Regassa Dukele
    - Able to push 3-bit ADC work on schematic level
    - Started working on OpAmp layout

Pending Issues

- How to actually perform the MAC operation with ReRAM cell - is it even possible with the simplified model we are given?
- Creating a layout of ReRAM device that passes both DRC and LVS checks

Individual Contributions

Team Member	Individual Contributions	BIweekly Hours	Total Hours
Joshua Thater	Got a response on how to write/verify write for 1T1R cell and began making final documentation	5	85
Aiden Petersen	Driver implementation and bug fixed in the digital behavioral model.	6	74
Matt Ottersen	Confirmed layout of Op-Amp Works	6	74
Regassa Dukele	Get 3-bit ADC to work on the schematic level	6	78

Plans for the Upcoming Weeks

- Joshua Thater
    - Finish writing up the documentation for the whole analog process flow.

        - How to set up environment
        - How to set up tools
        - How to use tools
        - How to push design through tools
    - Test write test on 1T1R cell and verify that write occurred
    - Ask more questions on 1T1R cell in Slack, namely how to perform MAC computations
- Aiden Petersen
    - Get analog model functioning and run tests to ensure digital behavioral model is working properly.
- Matt Ottersen
    - Work on 1 bit ADC layout and simulations
    - Work on Transimpedance Op-Amp simulations
- Regassa Dukele
    - Complete the layout of the Opamp and perform a post-layout simulation to validate the design
    - Keep working on ADC layout